MN EMC Event
Sept 2023

SIPI, EMC and the Edge of the Cliff
Lessons from a Long Design Career

John Severson, PE
ESDI

Electronic & Software Design, Inc.

- John R. Severson, PE
- President and Principal Engineer, ESDI
- 35+ years designing electronic circuits, systems PC boards, RF, Design for EMC, and software
- Broad experience in many markets
  - Airborne Electronics
  - Analog/Digital Instrumentation, Metrology
  - Medical Image processing and graphics
  - CCTV, Analog and digital audio, video and security
  - Adaptive technology for persons with disabilities
  - Agricultural IoT, specialty RFID, and RF modules

Electronic & Software Design, Inc.

ESDI Expertise

- Circuits, systems, and PCBs with high speed logic, Analog & mixed signal, wireless, video, CCD/ digital imaging, graphics, LCD display controllers
- Embedded Microcontrollers and Linux Software and recently IoT focused.
- Design for EMC and Signal Integrity, RF Modules integration, RFID systems
- SolidWorks (3D) and Altium Designer

Today's Presentation

- Look at SIPI and EMC from a Designer's perspective
- Tell a Few Stories
- Review some Technical Details – see my second presentation for more details
- Offer some Lessons from my career

SI, PI and EMC – From a Designer's Perspective

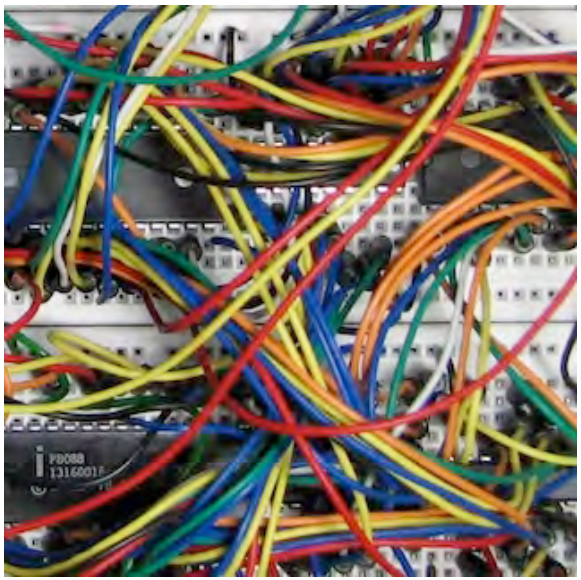
- As a ***designers***, we must be concerned with all three of these. Put simply our designs must:

  - ✓ **meet Specifications**
  - ✓ **work** (and **keep working in the real world)**
  - ✓ **pass compliance tests** needed for where it's going to be sold.
  - ✓ **meet timeline** and **cost** and **supply chain** constraints

SI/PI and EMC – Informal Definitions

- **SI – Signal Integrity**
  - Getting the **signal** from the **source** to the **destination** (load) without unacceptable deterioration.
- **PI – Power Integrity**
  - Getting the **power** from the **source** point to the **destination** (use point) without unacceptable deterioration.
- **EMC – Electromagnetic Compatibility**
  - Getting the product to deliver its **specified function** *and* **performance** without causing **interference** to or being **susceptible** to interference from other devices.

SI / PI / EMC – The obvious



✗

Might work on the bench if you are really lucky (and don't make measurements)

✔

High speed, mixed signal SOC BGA, DDR Ram, LVDS display, 20W switching Supply
High Integrity PCB is a MUST!

EMC and SIPI are Closely Related

- **Poor Signal Integrity** will usually **radiate** – uncontrolled signals go *somewhere*
- **Poor EMI/EMC** techniques usually lead to **poor Signal Integrity** – uncontrolled return paths lead to *crosstalk and timing issues*.
- **Poor Power Integrity** can lead to poor **EMC** and poor **Signal Integrity** (not to mention **function**) - Power and ground *are at the heart of a design*.

Signal Integrity Trends

- **High Speed**
  - **Rise Times** in **picoseconds** range
  - **Clock Frequencies** well into **GHz** range
  - **Data Rates** in **10's** of **Gbps** and beyond
  - **Analog Bandwidths** in **GHz** range
- **Shrinking Dimensions**
  - Very **high density and speed** Integrated **circuits** and PC Boards
  - Very **high density** and **high speed cables**

The “Real” (but inconvenient) World

- All "**components**", traces, planes, etc. are really distributed parameters and EM fields
- As Scale changes relative to values, the **parasitics** (the “**hidden schematic**”) and distributed effects can take over.
- No such thing as “**Ground**” – just conductors and **reference planes / points**
- The **Time Domain** is the only “real” domain

A Story from SI History

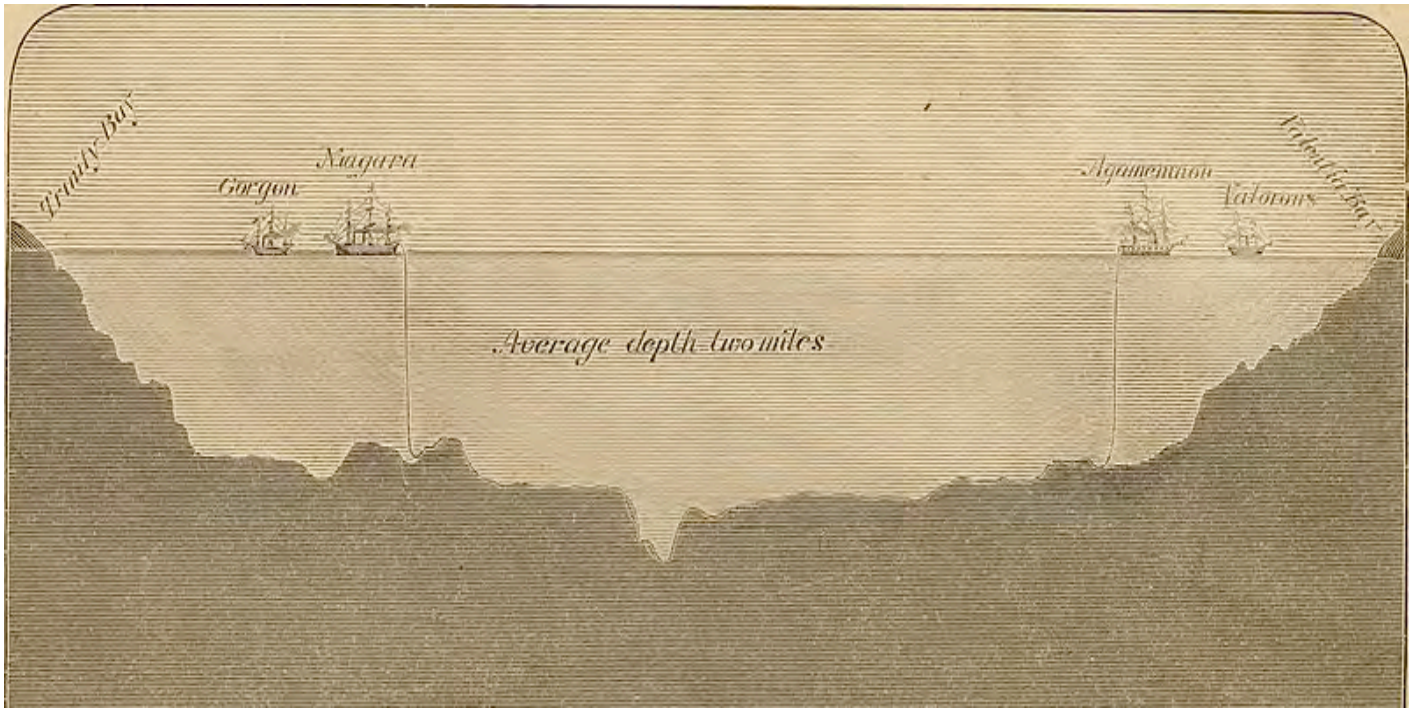
- **Signal Integrity** is NOT a new topic. It's been an intimate part of electrical and electronic engineering for centuries!
- It has always been a matter of understanding the effects of the **scale.**
- I want to tell a story about **how we got to today**…

An Epic failure of Signal Integrity…

...The First Transatlantic Cable – Completed 1858

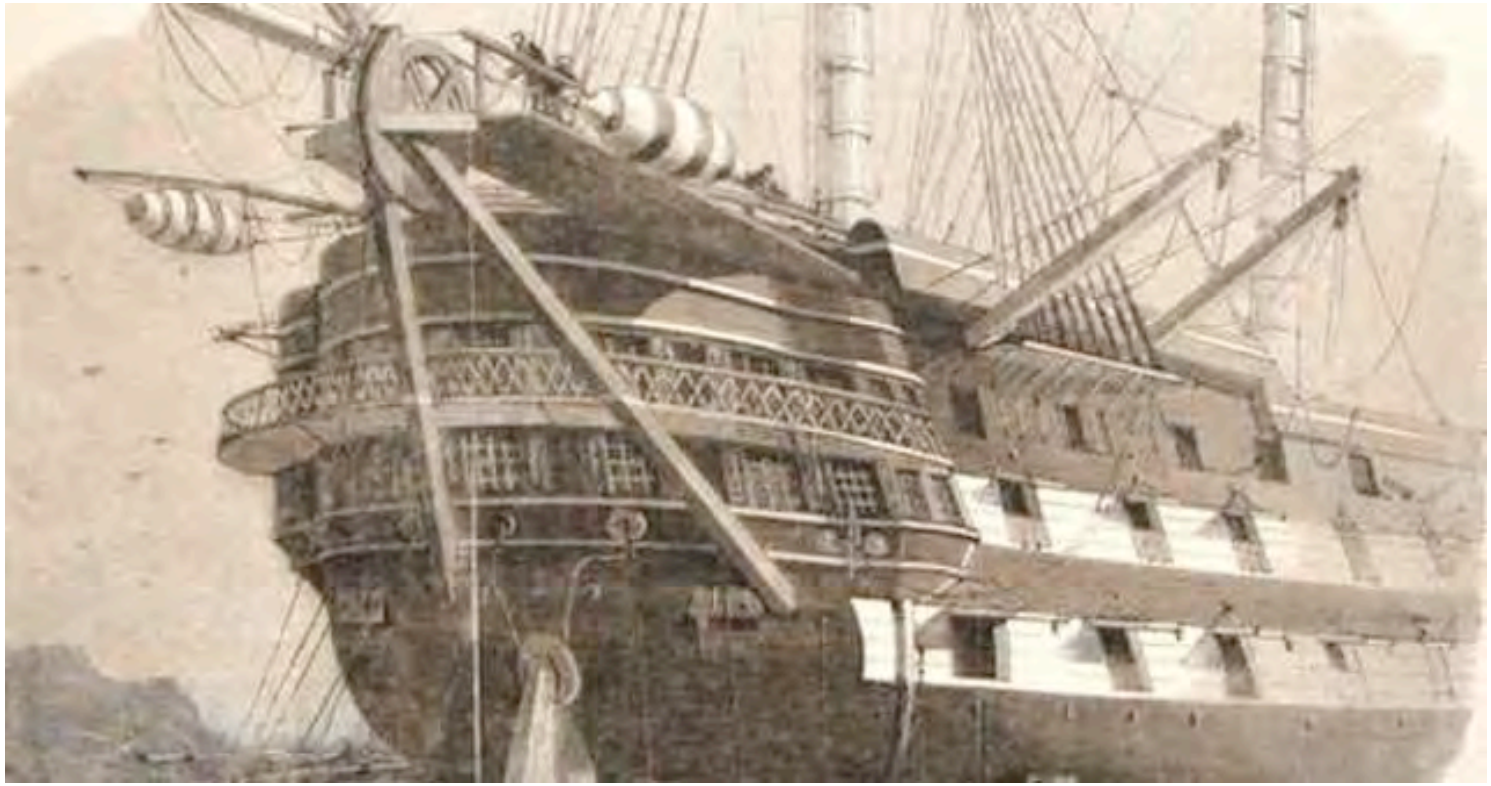
Public Domain, via Wikimedia Commons

It was an Epic Undertaking



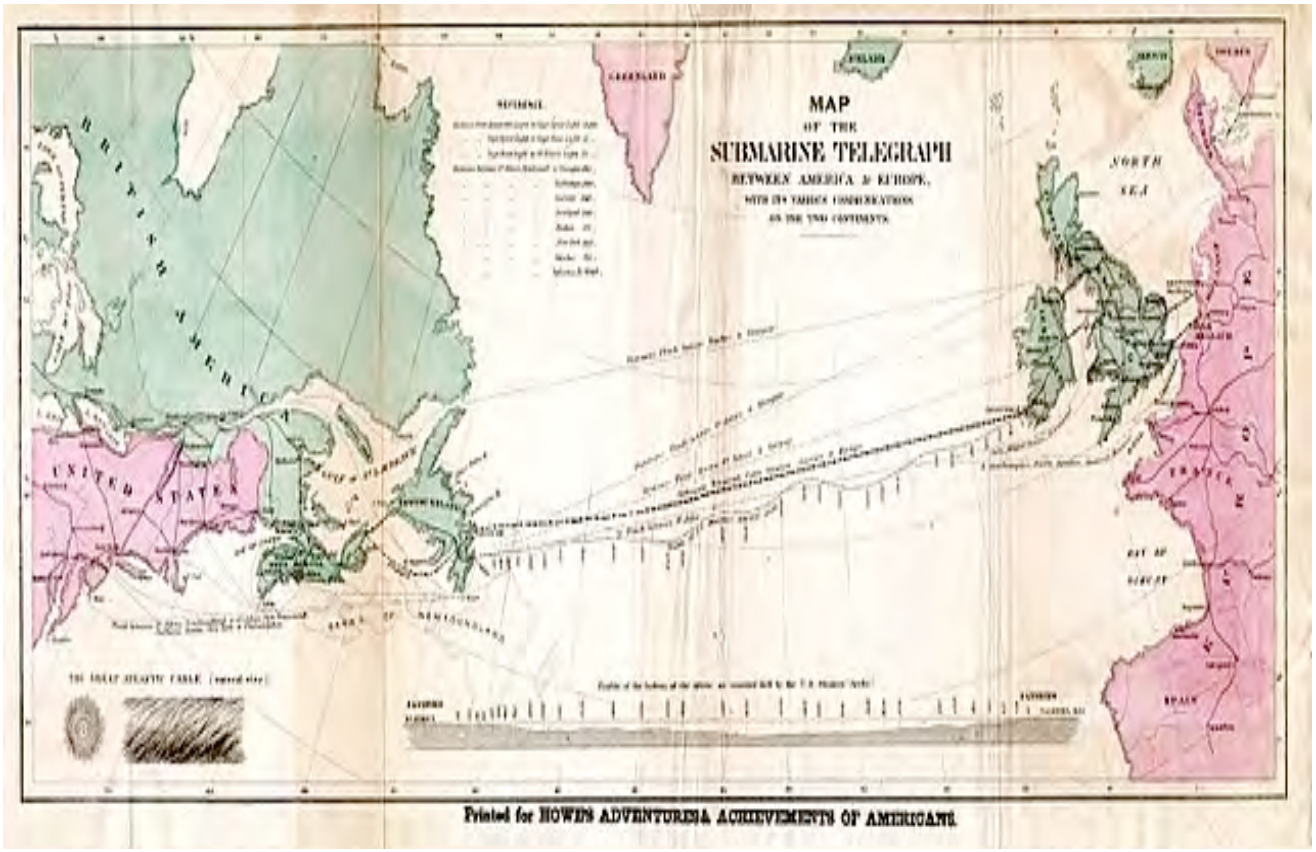
- Laying a 2500 nautical mile long cable on the sea bed in 1858 was no small task.

It was an Epic Undertaking



It took 3 attempts to lay the cable, multiple ships, 2 years, and the cost was outrageous.

The Cable



The Cable

- Just over 1.5" in outer diameter
- Outer casing of Iron wires
- Inner conductor 0.083" diameter Cu
- Insulation: Gutta Percha (a natural rubber)
- Put up in 100 mile reels

Terrible Performance…

- Intended to be similar to other telegraph cables of the day
- It took **16 hours** to transmit a 99 **word message** from Queen Victoria to President Buchanan (**Data rate** achieved – **0.1 word per minute)**
- The **signal** on the receiving end **was so weak** it required a sensitive **Mirror Galvanometer** movement to read the signal. (Invented by Engineer **William Thompson)**.
- The **Dots and Dashes were so blurred** that each word needed to be repeated and confirmed multiple times just to get through.

...And met a **painful end**

Chief Electrician (Engineer), Edward Orange **Wildman Whitehouse**

…tried cranking the operating **voltage** to **2,000 volts*** in hopes of speeding up the data rate, and the stopped working altogether.

Public Domain, via Wikimedia Commons

*Estimated peak voltage, depending on various accounts; Correction: Whitehouse's title was Chief Electrician not Engineer..

What Happened?

- Mechanical weaknesses?
- Poor insulation?
- Voltage Drop?
- Signal Degradation in the very long cable (dispersion, attenuation, etc.)?
- Water incursion and effects -- reflections due to flaws? Losses due to surrounding water?
- Note: Maxwell's equations not published until 1861/62/65/73 (even in their pre-vector form)

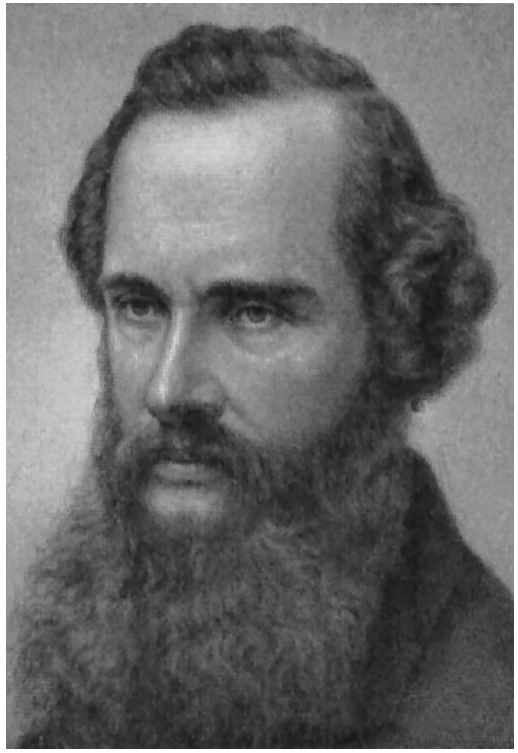
Perhaps all of the above, but regardless, the lack of a robust understanding of the signal degradation was problematic with respect to data rate

What Was Next?

- A board of inquiry **blamed Wildman Whitehouse**. This might not have been entirely fair, but at least with a "known cause" they were willing to continue to raise funds.
- (Whitehouse took "early retirement")
- Some of the best minds of the day worked on the problem…

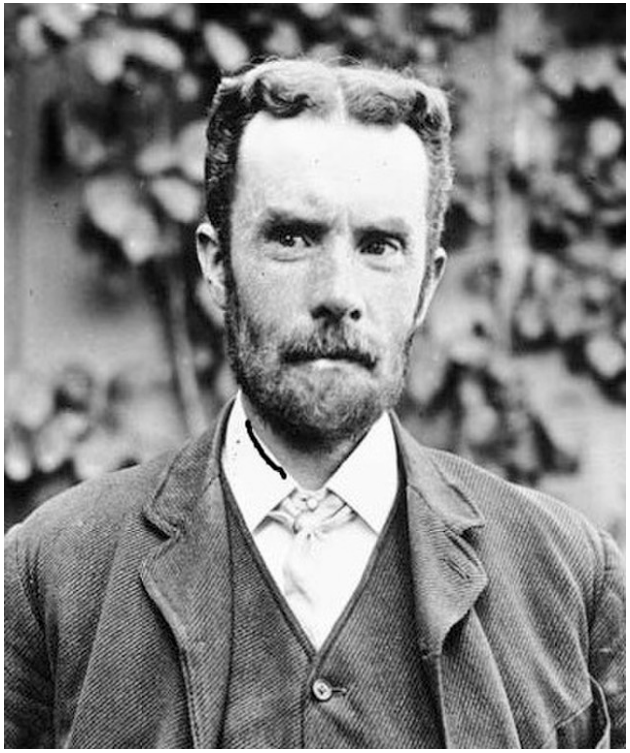
The actual cause of the failure is debated and not all agreed that Whitehouse was at fault. Some accounts suggest the cable was doomed regardless of Whitehouse efforts to repair the poor speed.ii

Signal Integrity Pioneers



William Thompson
(Lord Kelvin)

James Clerk Maxwell



Oliver Heaviside

Signal Integrity Pioneers

- **William Thompson** (who we now call Lord Kelvin) was involved with the first cable and then the second.
- **Maxwell** publishes early forms of equations in 1861/62 and 1865, and then publishes "**A Treatise on Electricity and Magnetism**" in 1873.
- **Oliver Heaviside** read Maxwell's Treatise in 1873 and helped develop **Transmission Line Theory** (also known as the **Telegrapher's Equations**, and **Transmission Line Models**
- **Oliver Heaviside** later reformulated Maxwell's Equations as the Vector field equations we are familiar with today.

A Brief Epilogue to the story

- The **first** redesigned, **successful Transatlantic cable** was completed in **1866** and it achieved a much better data rate (ca. 8 wpm)
- It wasn't until **the 1950's** that an audio (**telephone**) cable was completed - when the technology for **submerged signal repeaters** became possible.
- The **Lessons** from the **first cable** and the work of Michael Faraday, Lord **Kelvin**, **Maxwell**, **Heaviside,** and many **others** form the basis of how we analyze RF, EMI and the use transmission lines even today.

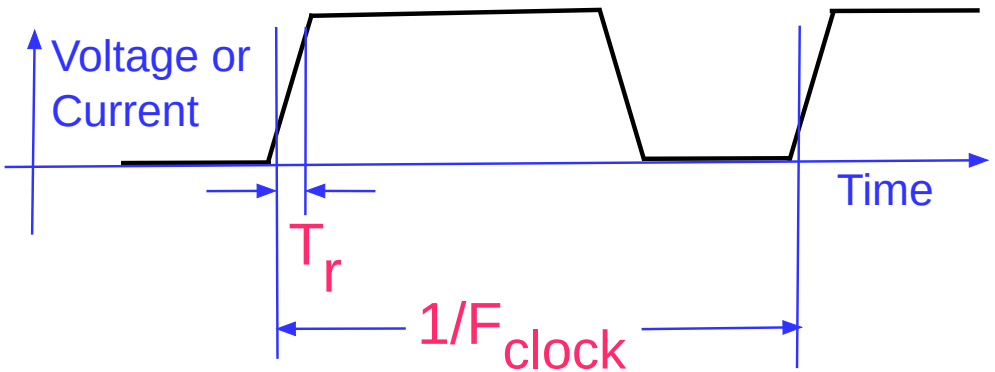
The Edge of the Cliff

- At **30 feet away**, you can step quickly and **without a lot of care**.
- At **3 feet away**, you need to **pay attention and slow down** a bit
- At **3 inches away**, you need to carefully **measure and test each and every step**.
- Most projects have a few key issues which **must be close to the edge**. Keep the **other issues far away** and spend enough time with the "**zoom lens**" to make sure you can tell the difference.

Some Key Common Considerations in SI, PI and EMI

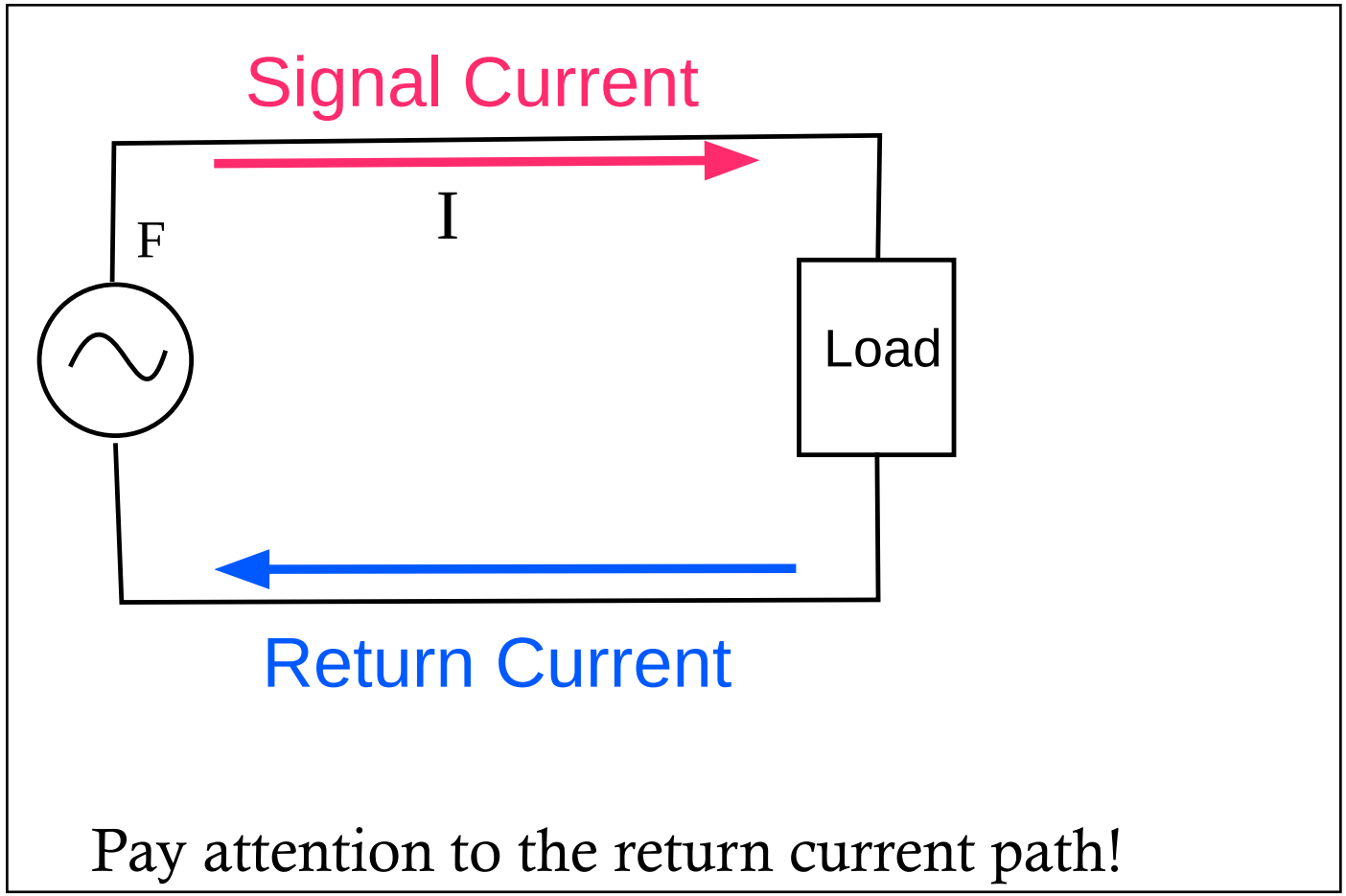
- **Rise Times** and **Frequencies** (including harmonics)
- **Signa**l and **Return Path**
- **Transmission Lines**, Impedance, Terminations and Reflections
- **Crosstalk** and **coupling**
- **Ground, Power** Integrity and the **PCB Stack up**
- **Timing, jitter and skew**, simultaneous **data transitions**

Clock Frequency, Rise Times, and Scale



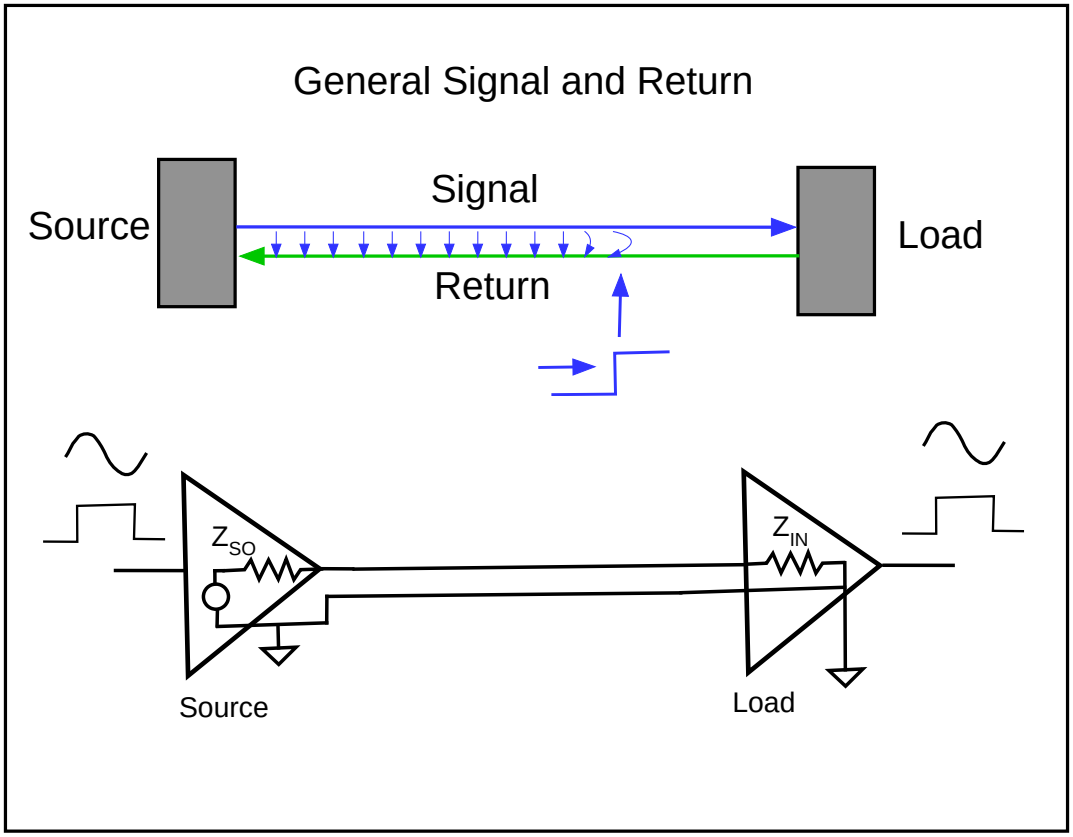
Clock Frequency	Rise Time (1/10)	Wavelength λ (m)	10th Harm	λ /10
1 MHz	100nS	300 m	10 MHz	30 m
10 MHz	10nS	30 m	100 MHz	3 m
100 MHz	1nS	3 m	1 GHz	30 cm
1 GHz	100pS	30 cm	10 GHz	3 cm
10 GHz	10pS	3 cm	100 GHz	3 mm

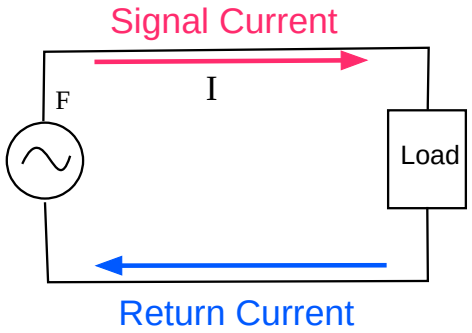
The Signal: Every Signal has a **Signal Path** *and* a **Return Path**.



Pay attention to the return current path!

Is it a “Transmission Line”





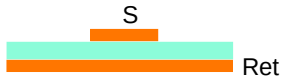
Some Common Uniform Transmission Lines

Cables

- Coaxial Cables
- Twisted Pair
- Twin Lead
- Waveguide

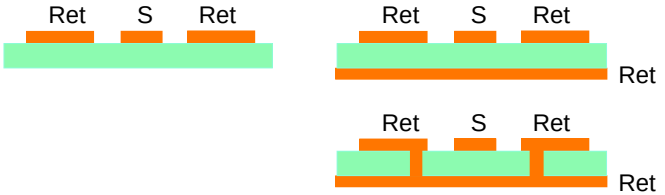
In PCBs (planar T-lines)

- Microstrip



- Stripline

- Coplanar Wave Guide



Controlled, **constant impedance**. The characteristic impedance Zo doesn't vary over the length of the line. Can be differential or SE

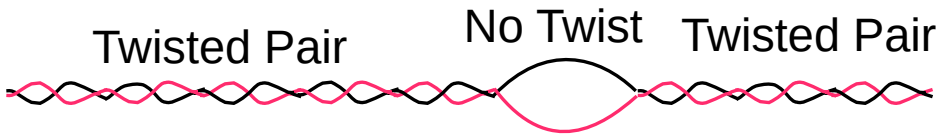
Impedance

- The ratio of **Voltage** to **Current**
- **AC / RF** Impedance **Z = R + jX**
- **Average** (or net) **Impedance**: (depends on frequency)
- **Instantaneous Impedance**: V/I at a particular point in the circuit (e.g., along a PCB trace or transmission line).
- **Characteristic Impedance of Transmission Line**: Z_0

Reflections and Terminations

- Any **impedance mismatch** (from Z_0) will cause a **reflection** in a transmission line.
- **$Z > Z_0$**, the **reflection** will be **positive** in sign.
- **$Z < Z_0$**, the **reflection** will be **negative** in sign
- Any **change in impedance** along the way will **cause a reflection**..
- **Reflections** *will* **interfere** with **signal integrity**
- If **$Z = Z_0$**, **NO reflection**

Example Impedance Changes



PCB Change in Trace Width over ground plane

PCB Trace over GAP in ground plane

- Avoid Impedance changes, including a gap or flaw in the return path
- If rise time >> the the propagation time, effect is small
- Rule of thumb: **problem if Tp < 20% of Tr**

Example: Scale vs. Rise Time: **Remote PTZ control**

The Challenge:

- Spec required **real time interactive control** of multiple channels on a single pair and installation
- Spec *precluded* **terminators** or special cables (needed to work with existing untwisted wires).
- Cabling exceeding **1000 feet** was required.
- A conventional approach **would NOT work without terminations** due to the required data rates, cable length and reflections

Remote PTZ control using Long Un-terminated Cables

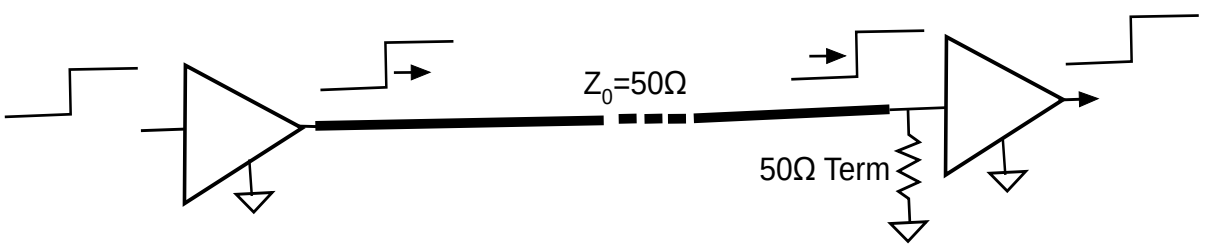
The Solution:

- Use a *very* slow rise time (well below the critical length) to prevent reflections from being problematic.
- Use high efficiency data encoding to reduce the required data rate, at the expense of SNR
- Continuous update mitigated the SNR so that any errors were immediately corrected

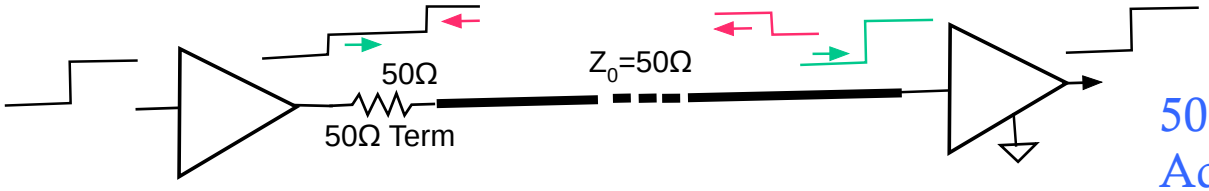
Take Aways:

- **Working *with* the scale** and finding a solution **which fits within the scale** can avoid the "cliff."
- **EMI issues were nil since** the **rise time was *very* slow**. Unshielded, untwisted, un-terminated wiring worked well
- Very **robust** and **simple** for the time.
- **Edge of Cliff Avoided**

Review of Terminations

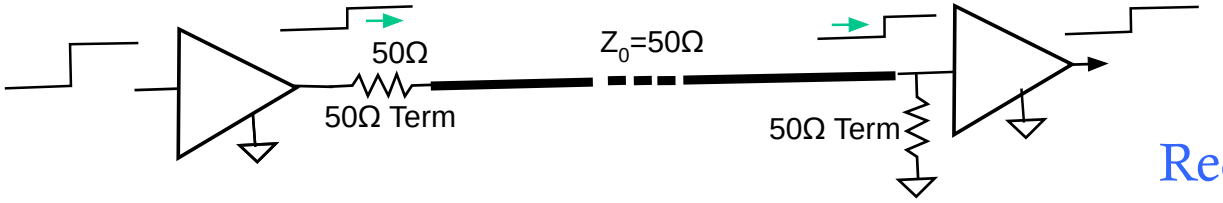


Parallel Termination



Series Termination
(Back Matching)

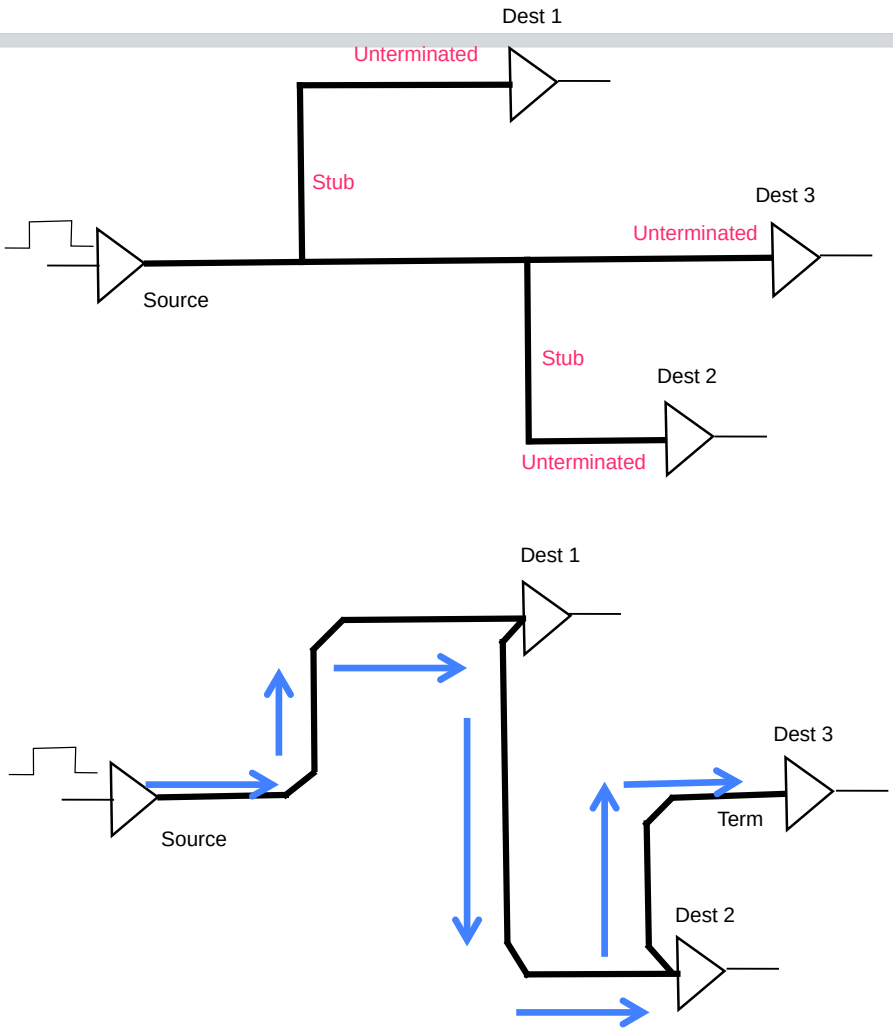
50% pulse; 50% reflection; Add at load; No reflect at source



Dual Termination
(Combination) –

Requires 2X gain

Reflections and terminations



"**Stubs**," even short ones can wreak havoc on an otherwise well done line.

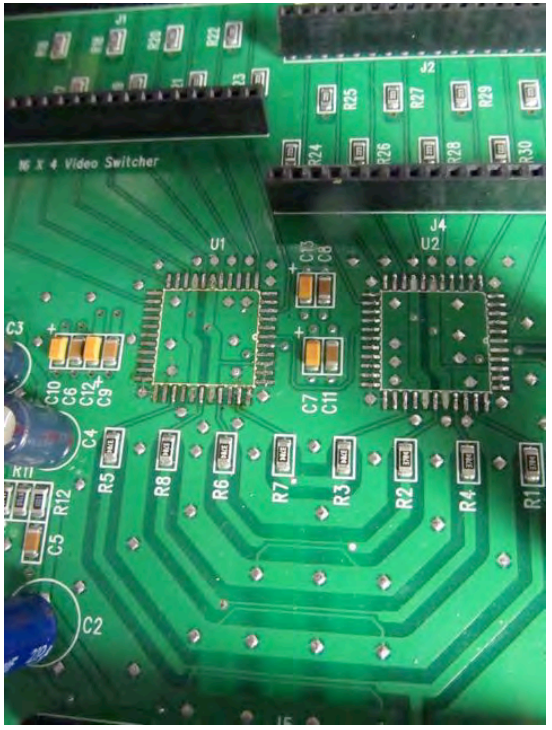
Reflections from the un-terminated **stubs** will bounce around back and forth causing "glitches."

A well designed signal route for **multiple end-points** has **one source** and **one terminated end-point**. All other "drops" **are daisy chained** as a single route.

Example Difficult Terminations: **Modular 16 x 4 Matrix Switcher**

The **Challenge**:

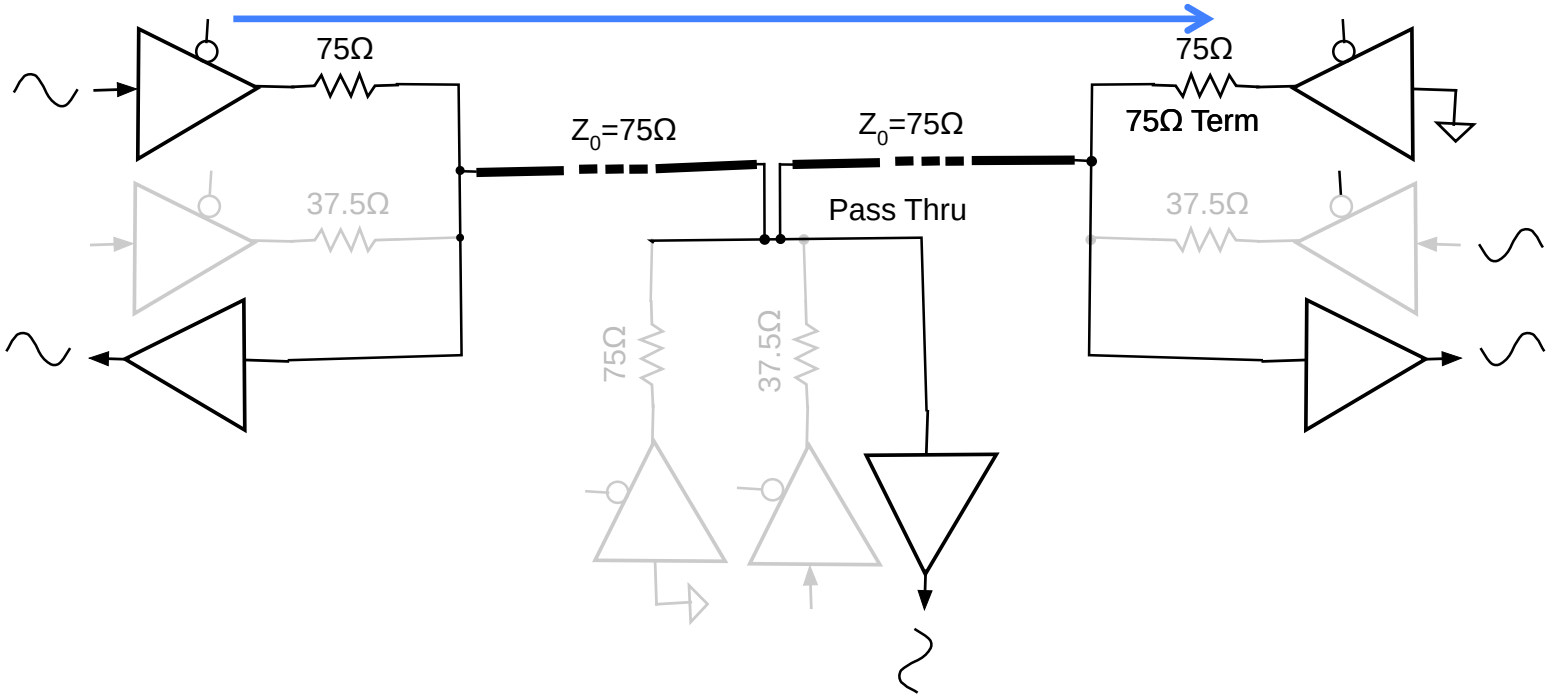
- Analog Video **Switching Matrix** Bus with up to 8 Switchers and 10m of combined 4 channel output bus length.
- Spec required **no manual terminations** – Must be fully self sensing and auto-terminating
- Simple plug-in cables – **no special installer skills** or configuration
- High **SNR** (Signal to Noise) and **low Crosstalk** required
- **2 layer boards** specified – Difficult to accomplish **X-talk and Zo** Continuity
- Must Pass **FCC** and **CE** tests including **EFT, ESD, EMI**, etc.



PCB showing Coplanar Waveguide lines (2 layer)

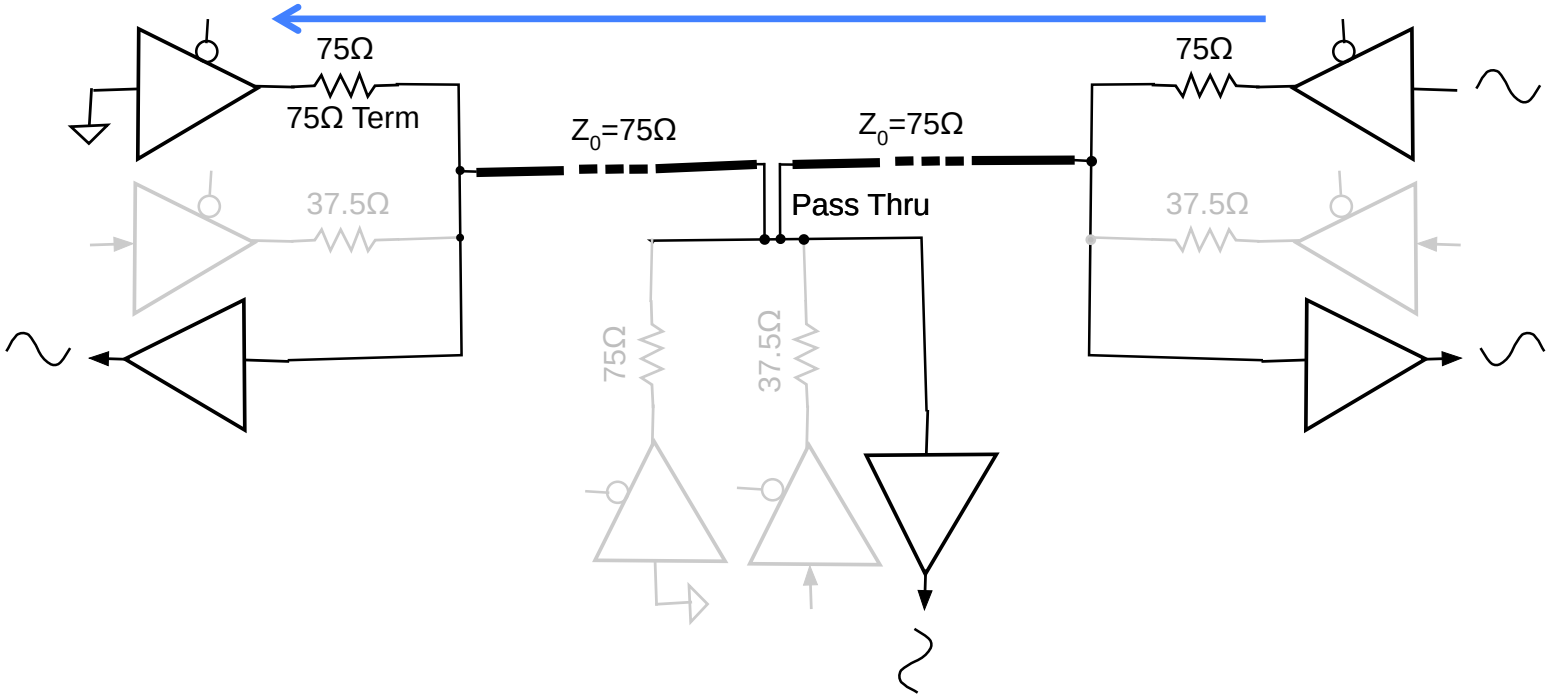
Solution: Multi-drop Bus

Left End point Drives – Right End Point Terminates



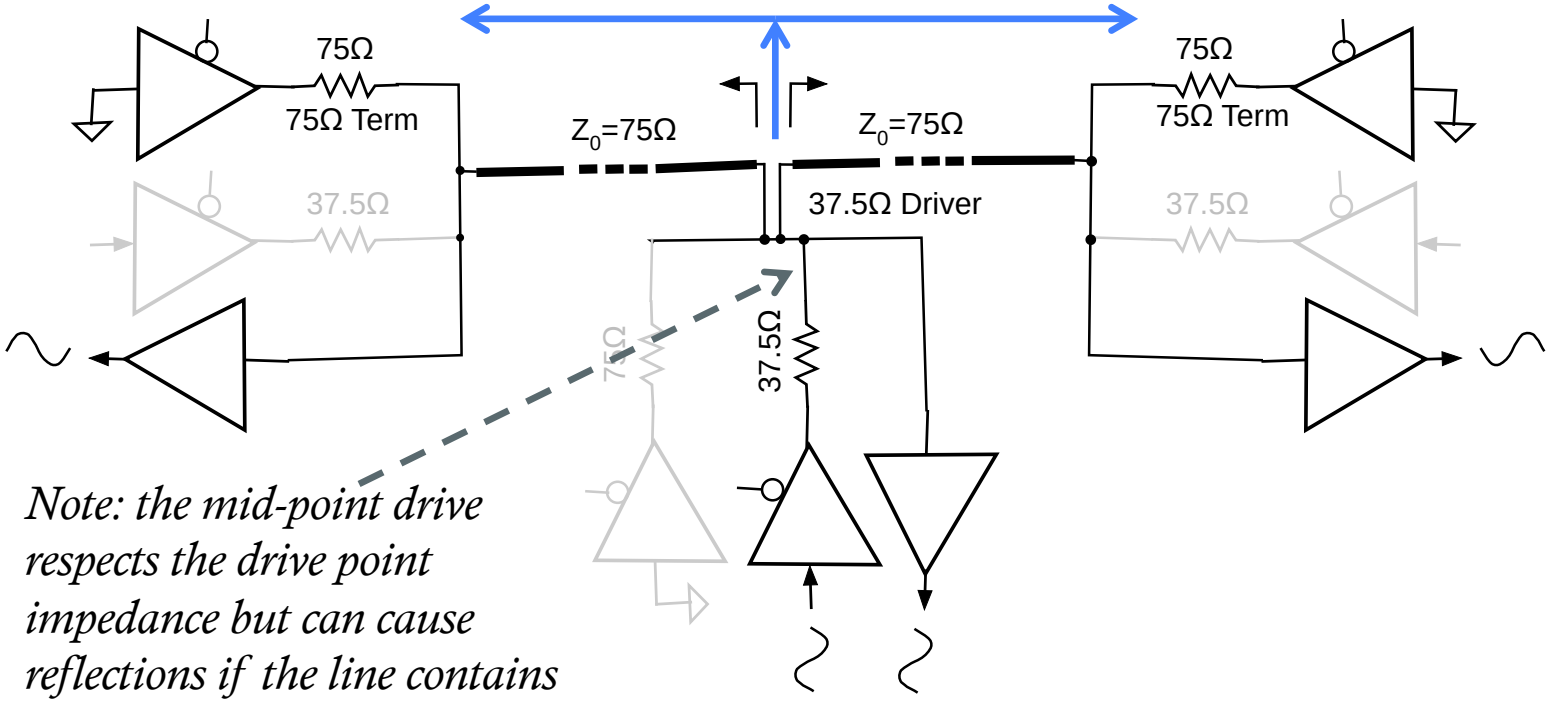
Solution: Multi-drop Bus

Right End point Drives – Left End Point Terminates



Solution: Multi-drop Bus

Mid point Drives – Both End Points Terminate



Note: the mid-point drive respects the drive point impedance but can cause reflections if the line contains impedance flaws longer than 20% of Trise.

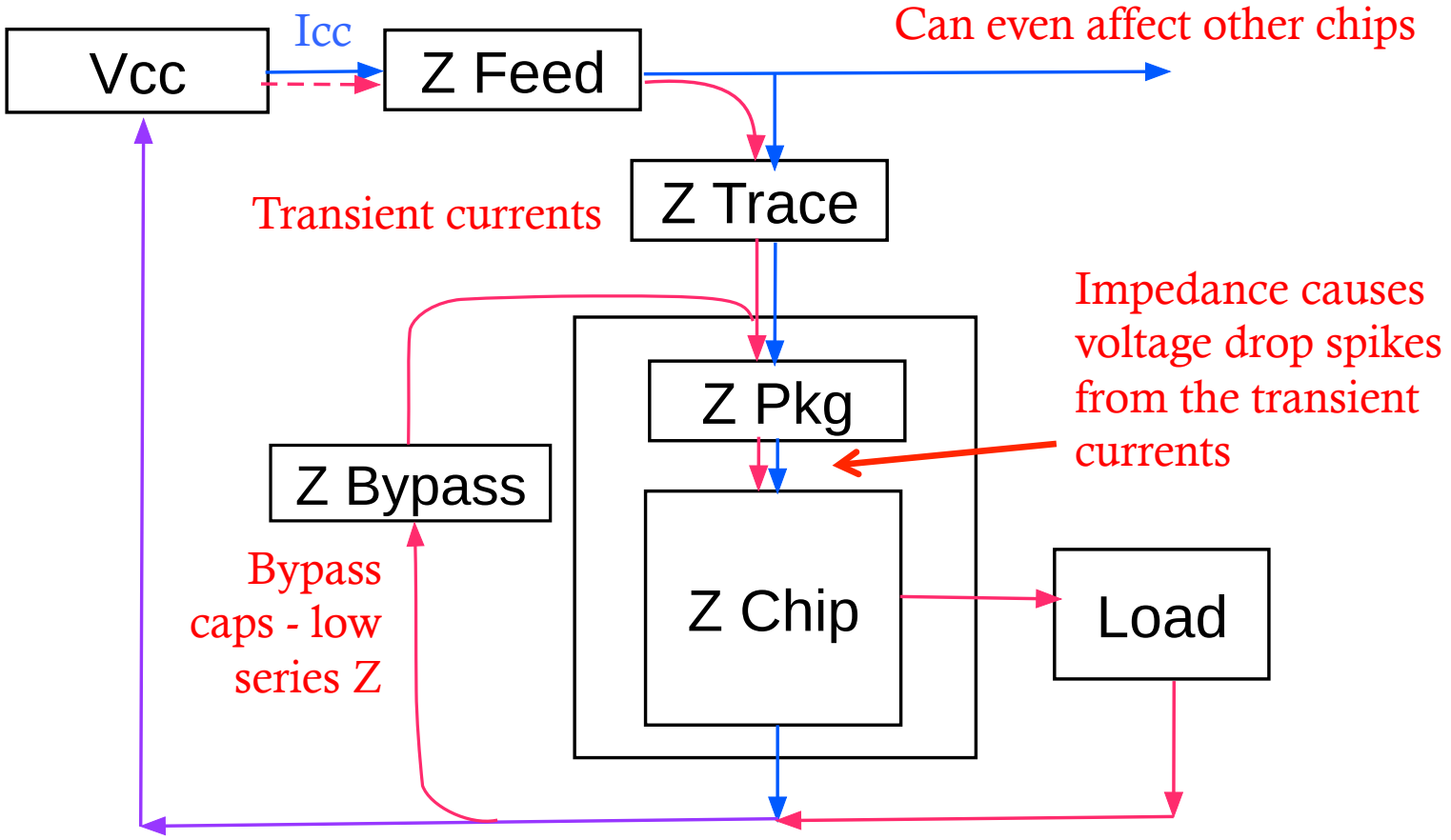
Take Aways:

- Series / parallel (**dual**) **Termination**, Parallel **Split**
- **High Integrity Drivers** can also be high integrity **active terminators**
- **EM simulation was unavailable**, so a **simple prototype** PCB of just the **Coplanar waveguides** bracketing the approximations was made and tested to get the best design.
- Note: **Spice simulation** was used extensively to model **drivers**, **terminations,** the **bus** and **protection circuitry**
- **Worked very well** and **passed all tests**.
- **Edge of Cliff Avoided**.

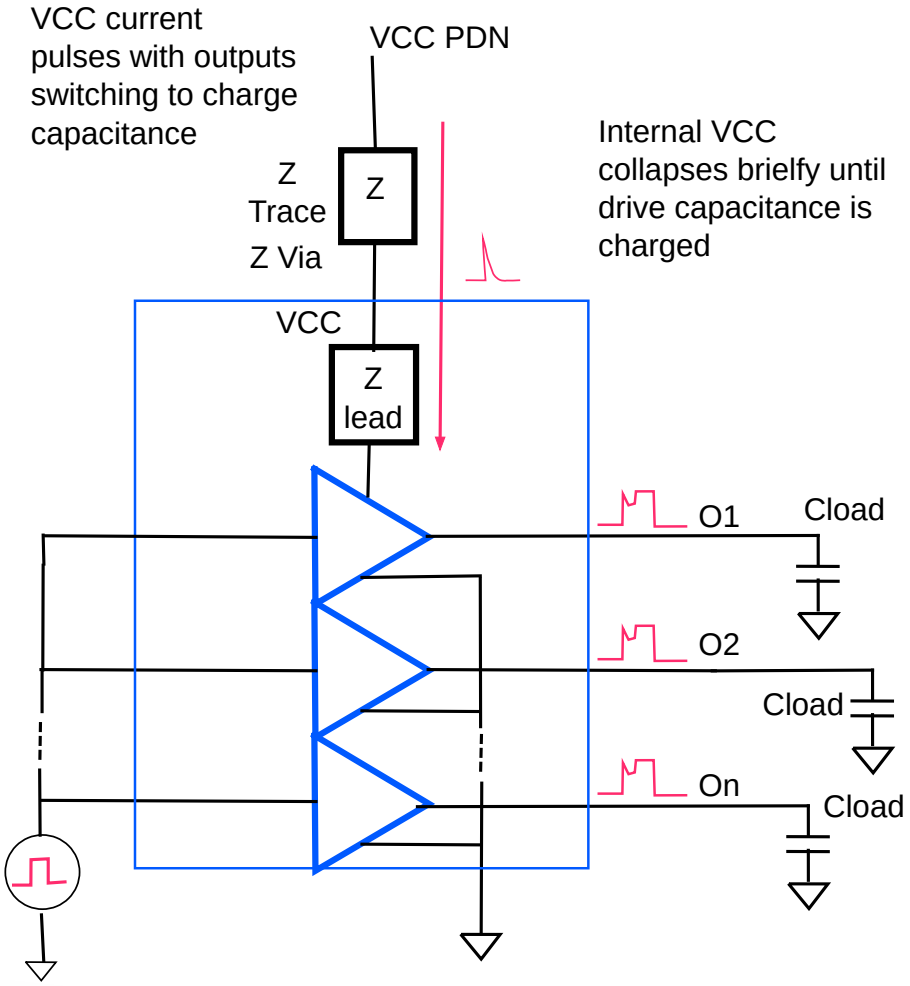
Crosstalk

- **Crosstalk** is the **unintended coupling** of one signal into another.
- **Crosstalk** can manifest as **noise**, data or measurement **errors**, clock "**glitches**," and/or radiated and conducted **EMI** – V, mV, uV
- **Power supply** issues can be a **special case of crosstalk**.

Power Distribution Network and Bounce

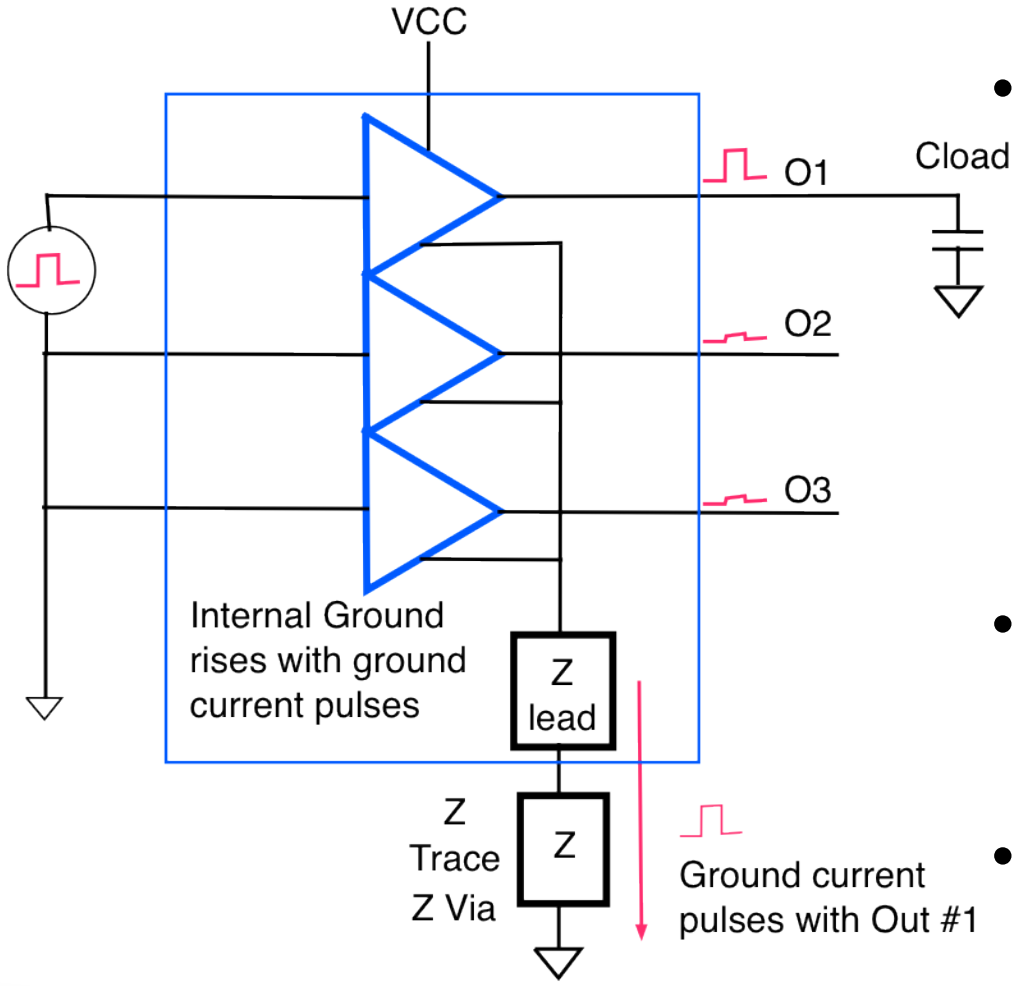


Power Impedance, Bounce, and collapse



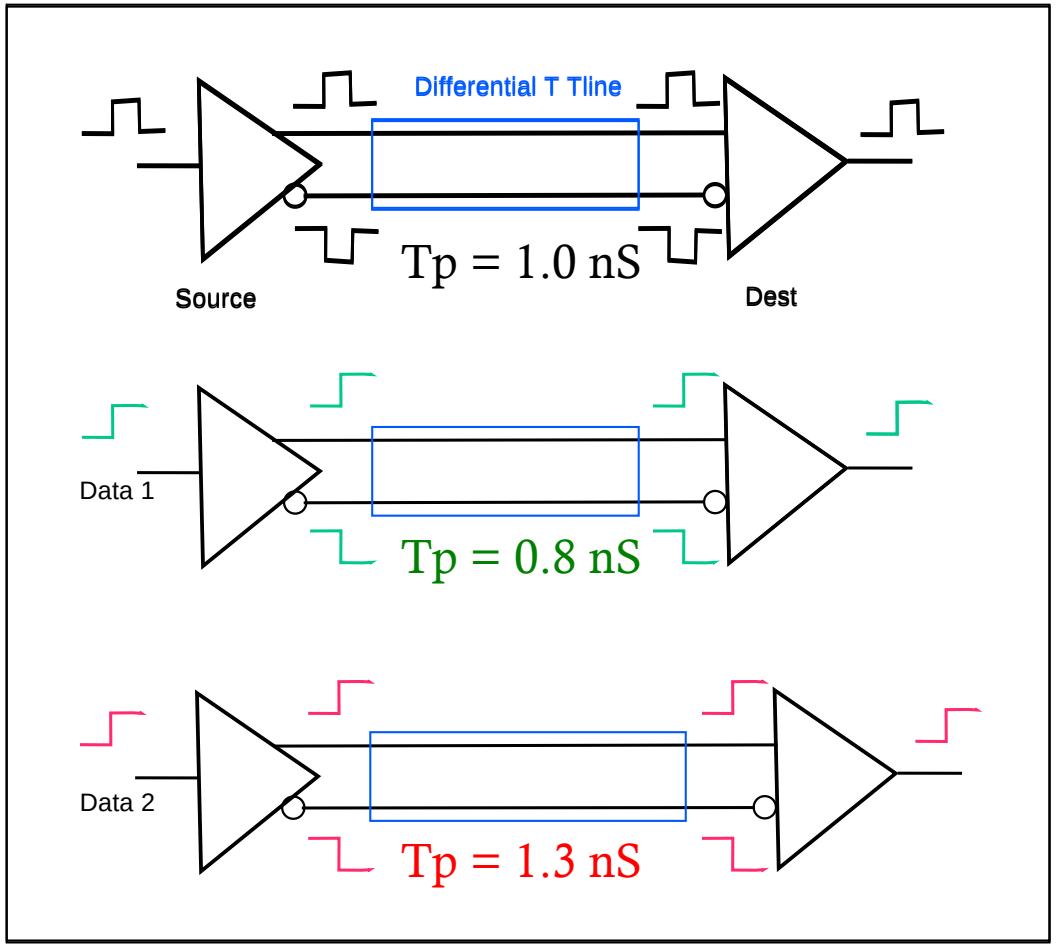
- VCC drop -- **couples to outputs**
- May cause **logic failures**
- May cause a **larger collapse** of VCC
- Low Z BYPASS caps are a **must**

Ground Impedance and Ground Bounce



- Switching currents **are coupled to other outputs** (and other circuits) through common impedance
- **Low speed** signals still **can contain RF**
- Must keep **ground impedance low**!

High Speed Delay and Skew



- **Transmit** as a **pair** -- **Receiver** only cares about the **difference.**
- Requires **plus** and **minus** to **arrive** at exactly the **same time**
- If arrival time isn't exact, the output is **distorted**
- Any **Tp difference** in causes **skew** of signals (500 pS in example)

Cliff Unavoidable:

Controller for LCD Monitor With networked Media Player

- High speed digital mixed with precision analog – Processor, Video Signal processing, Graphics
- DDR Ram Interface
- LVDS display interface to cable
- 20W switching Supply
- Fast Digital and Analog Edge connector to Camera and IO / Media Board

Monitor had to **pass EMI tests** in a **plastic enclosure**

Controller for LCD Monitor With networked Media Player

The Solutions

- Use **careful partitioning and segmenting**;
- **Wall off** the very **"close to the edge" portions** and uncouple from other functions.
- Use very **careful 6-layer stack up** and **management of reference planes**
- **Follow the reference designs** where available;
- **Leverage previous experience** such as DDR, LVDS, etc layout and previous monitor controller designs
- **Simulate** critical and unknown portions as practical
- **Test, Test, Test** (especially for 3rd party portions)
- **Seek the advice** of an outside consultant on some issues and follow it
- Use an **internal Shield** and careful internal **chassis ground structure**
- Do **some EMI Pretest** before taking it to the test lab
- **Watch out for "pre-certified"** 3rd party items

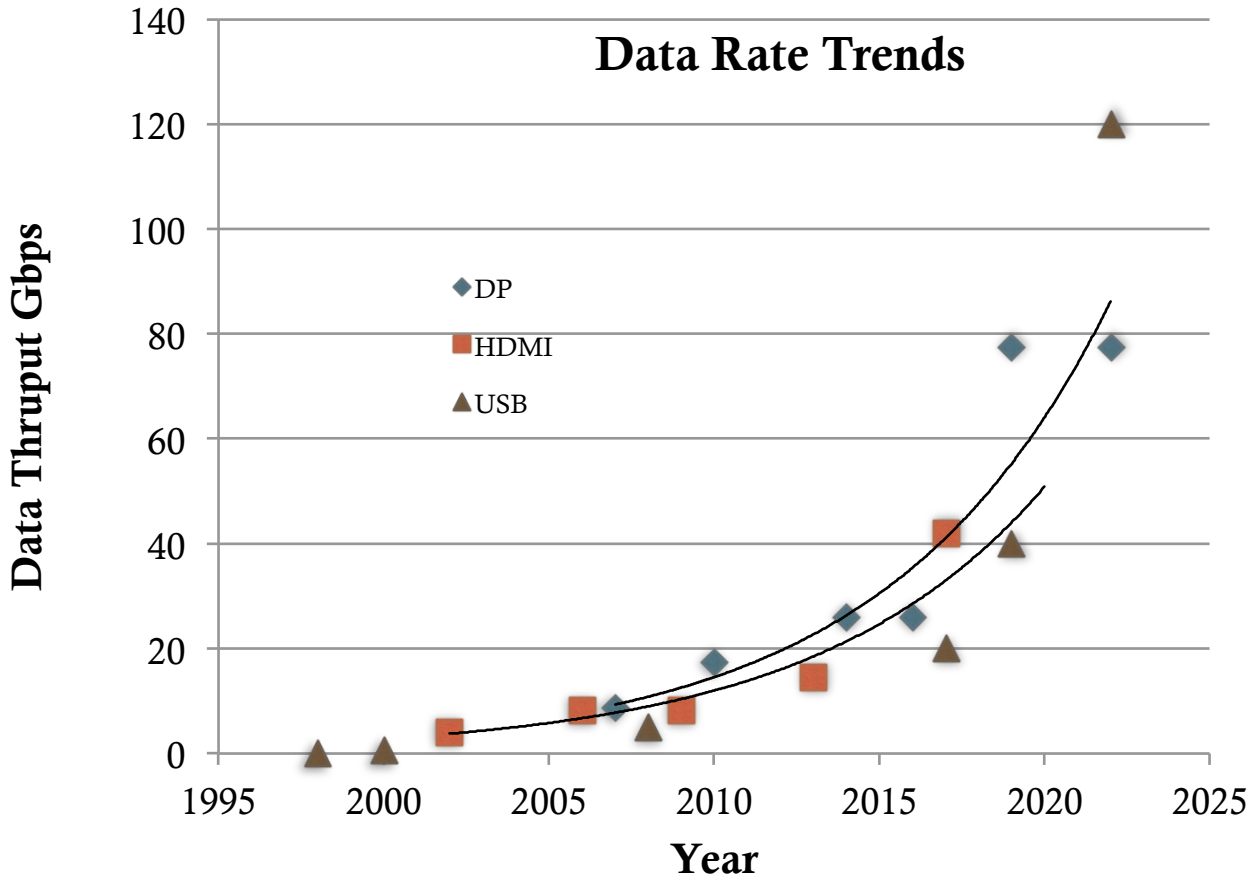
Take Aways:

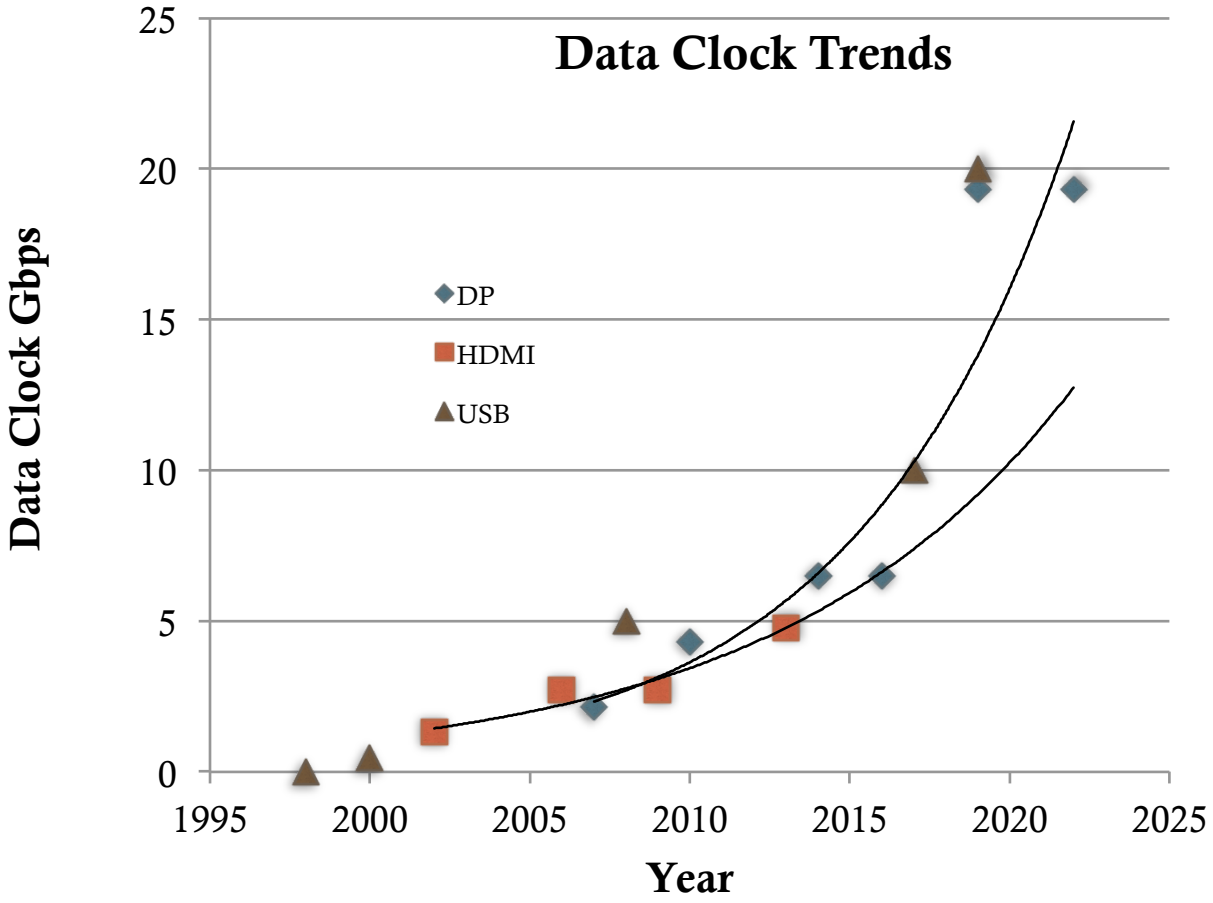
- Combining **high bandwidth Analog** and **High Speed Digital** ***is*** very challenging and **definitely requires great care and attention to details**.
- **High speed interfaces** like DDRx memory **require very special care** with timing and layout/routing
- Adding **switching power supplies** to the mix, especially higher power supplies adds another dimension.
- **Start** with the **Stack up** and expect a **2-sided board**
- **Edge of Cliff unavoidable**. Don't be intimidated, but **navigate with great care**.

The March toward the Edge

Some Data Interfaces over time…

- **Display port** 2007-2022, **HDMI** 2002-2019, **USB** 1998-2022
- **Needed for SI -- Good for EMI**:
  - High Speed, Low Voltage **Differential pairs** (from LVDS origins)
  - Increasingly **sophisticated encoding and clock / clock recovery**
  - **Twisted pair** cables (shielded) and **special connectors**
  - **Interfaces** including **drivers embedded in silicon**
  - **Adaptive Equalization**


Data Rate Trends
Data Thruput Gbps
Year
DP
HDMI
USB
0
20
40
60
80
100
120
140
1995
2000
2005
2010
2015
2020
2025


Data Clock Trends
Data Clock Gbps
25
20
15
10
5
0
1995
2000
2005
2010
2015
2020
2025
Year
DP
HDMI
USB

Where is the "Edge"

- Depends on **your** project and **specs** – Need to **zoom-in** and **calculate**.
- **Analog**: High SNR, low signal levels, wide bandwidth, High interference potential (SI)
- **Digital**: Fast rise times, Fast Data Rates (SI, EMI) – are you counting nH or pH?
- **Power**: High dv/dt and di/dt levels; High currents, voltage, power (EMI)
- **Experience**, **Time** line and **budget**, **Risks**, Access to **tools**

Simulation

- **Circuit /SI Simulators**
  - Spice (LTSpice, pSpice, Hspice, TI pSpice etc.)
  - Various Mixed Signal and SI (e.g., EDA built-ins)
- **EM Field Solvers**
  - 2D Field Solvers
  - 3D Field Solvers
- **Models** can be problematic
  - Availability issues (e.g., Spice, IBIS – proprietary)
  - Be sure to validate

Summing up…

- **Identify** the **Edge(s) of the cliff** in your design
- Use a "**Zoom lens**"
- **Focus** on the **areas** where you must be **near the edge**
- **Understand** the **scale** (electrical vs. physical)
- Transmission line **Theory works**
- Avoid **Impedance Discontinuities**
- **Good SI** usually means **better EMI**

Summing up…

- **Simulate** where you can, and **focus on the cliff's edge**
- **Measure** to **confirm** designs, models, and simulations
- "If it's **not tested**, it **doesn't work**."
- Failing to control the **return path** *will* result in **poor SI, poor PI, and poor EMC.**
- **EMI** – Frequency - also think in the time domain
- **SI** – Time - also think in the frequency domain.

Questions?

Thank You!

Stop by the ESDI table for more Info

Electronic & Software Design, Inc.

6110 Blue Circle Drive, Ste. 245
Minnetonka, MN 55345

John R. Severson, PE
952-935-9459
js@esdimn.com esdimn.com

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